PROGRAM-CONTROLLED UNIT AND METHOD FOR IDENTIFYING AND/OR ANALYZING ERRORS IN PROGRAM-CONTROLLED UNITS

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Cross-Reference to Related Application:

This application is a continuation of copending International Application No. PCT/DE00/02956, filed August 28, 2000, which designated the United States.

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Background of the Invention:

Field of the Invention:

The present invention relates to a program-controlled unit having elements which can be connected to form one or more scan chains, and to a method for identifying and/or analyzing errors in program-controlled units using scan chains.

Program-controlled units, such as, in particular, microprocessors, microcontrollers, signal processors and the like, and also methods for testing these have been known for a long time in a multiplicity of embodiments.

Program-controlled units with scan chains and methods for testing program-controlled units using scan chains allow program-controlled units to be examined particularly quickly and reliably for errors.

The scan chain elements are normally selected flip-flops or all the flip-flops in the circuit to be tested. These flip-flops can be connected to form one or more scan chains when testing the circuit which is to be tested. In this context, the flip-flops are connected one behind the other in series, with the input connection of a respective flip-flop being connected to the output connection of the flip-flop which is in series upstream of it, and with the output connection of a respective flip-flop being connected to the input connection of the flip-flop which is in series downstream of it.

Such a scan chain, more precisely its elements formed by flip-flops in the example under consideration, can be initialized relatively easily. This is because a signal applied to the input connection of the first flip-flop in the scan chain, more precisely the state of the flip-flop in question which arises in response thereto, is shifted onward from flip-flop to flip-flop with the timing of a clock signal applied to the flip-flops; with each clock pulse, each flip-flop in the scan chain adopts the state of the flip-flop which is upstream of it in the scan chain.

If the xth flip-flop in the scan chain needs to be changed to the state A, then it is necessary to apply a signal "only" to the input connection of the first flip-flop in the scan chain,

the signal allowing this flip-flop and the flip-flops

connected downstream to be changed to the state A, and x clock

pulses need to be applied to the scan chain (to all the flip-

flops therein).

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Conversely, the states of the individual flip-flops at a

particular time can be read sequentially on the last flip-flop

in the scan chain.

10   If the scan chain contains n flip-flops, then a circuit to be

tested is tested on the basis of the scan method as follows:

first, the circuit is changed to the scan mode of operation,

as a result of which the aforementioned scan chain is formed.

This scan chain is changed to a defined initial state by

15   sequentially applying n input signals and n clock pulses. The

scan chain is then broken up and the circuit to be tested is

briefly started up for test purposes. In this context, at

least some of the states of the flip-flops initialized at the

start change, and from correct operation of the circuit to be

20   tested it can be ascertained in which (nominal) state the

flip-flops ought to be at a respective time. If the flip-

flops are connected to form the scan chain again after a

certain time and have clock signals applied to them, data

representing the (actual) state of the flip-flops in the scan

25   chain at the time at which the circuit's test mode ended are

shifted out at the end of the scan chain (from the output

connection of the last flip-flop in the scan chain)

sequentially with the timing of the clock signals. If the

actual state of the flip-flops in the scan chain, ascertained

as described, is then compared with the known nominal state

5   thereof, this reveals whether or not the circuit to be tested

is operating correctly.

With suitable action, it is possible to identify almost any

errors in program-controlled units quickly and easily in the

10   manner described.

However, experience has shown that certain errors are not

identified in a circuit test carried out as described above.

This applies particularly to errors which arise only under

15   quite specific conditions. Such errors are, by way of

example, errors which arise only at a particular time after

the circuit has been started up in a quite specific

environment (for example errors which arise only approximately

30 seconds after the circuit has been started up at an ambient

20   temperature of -20°C and at a supply voltage of 5.3 V).

At present, such errors cannot be identified and analyzed, not

reliably at any rate. This is frequently the case even when

the circumstances under which the errors arise are known.

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Summary of the Invention:

It is accordingly an object of the invention to provide a program-controlled unit and a method of detecting and/or analyzing errors in program-controlled units, which overcomes the above-mentioned disadvantages of the heretofore-known devices and methods of this general type and which further develops the apparatus and the method such that it is also possible for errors such as arise only under certain circumstances to be identified and/or analyzed quickly and reliably.

With the foregoing and other objects in view there is provided, in accordance with the invention, a program-controlled unit, comprising a plurality of elements to be connected to form one or more scan chains; and in which, in response to a predetermined event during program execution, the program-controlled unit can change into a state in which selected ones or all of the plurality of elements are no longer able to change a state thereof.

In accordance with an added feature of the invention, the program-controlled unit has an On-Chip Debug Support unit configured to monitor for the occurrence of the predetermined event.

In accordance with an additional feature of the invention, a clock generator supplies respective units of the program-controlled unit with clock signals, and the program-controlled unit is changed to a state in which selected ones or all of

5   the elements that can be connected to form scan chains can no longer change their state by deactivating the clock generator.

In accordance with another feature of the invention, an interface is provided that is suitable for configuring and/or

10   controlling parts of the program-controlled unit provided for identifying and/or analyzing errors that have occurred in the program-controlled unit from outside the program-controlled unit.

In accordance with a further feature of the invention, the

15   interface is configured for setting the predetermined event and a reaction of the program-controlled unit to the occurrence of the predetermined event.

20   In accordance with again a further feature of the invention, the interface is configured to prompt for or effect connection of the elements to form a scan chain, and also to read from and write to the scan chain.

25   With the above and other objects in view there is also provided, in accordance with the invention, an error

determination method in a program-controlled unit using scan

chains, that is a method for identifying and/or analyzing an

error indication. The novel method comprises reading the scan

chains after a predetermined event has occurred during

5   execution of a program by the program-controlled unit.

In accordance with again an additional feature of the

invention, in response to the occurrence of the predetermined

event, the program-controlled unit is changed over to a state

10 in which selected ones or all elements that can be connected

to form scan chains can no longer change their state.

In accordance with a concomitant feature of the invention,

there is provided a step of reading data obtained upon reading

15 the scan chains and comparing the data with data obtained when

the scan chains in an error-free program-controlled unit are

read under comparable conditions.

In other words, the invention achieves the objects as

20 respectively outlined in the device and in the method, namely,

-   in that, in response to a predetermined event during

    program execution, the program-controlled unit can change

    to a state in which selected ones or all of the elements

25 which can be connected to form scan chains are no longer

    able to change their state (cf. device); and

-    that the scan chains are read after a predetermined event

     has occurred during execution of a program by the program-

     controlled unit (cf. method).

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If, in response to a predetermined event during program

execution, the program-controlled unit changes to a state in

which selected ones or all of the elements which can be

connected to form scan chains are no longer able to change

10 their state, and if the elements which can be connected to

form a scan chain are then connected to form a scan chain and

the scan chain is read, the data obtained in the process can

be used to identify quickly and reliably even such errors in

the program-controlled unit as arise only under certain

15 circumstances.

Other features which are considered as characteristic for the

invention are set forth in the appended claims.

20 Although the invention is illustrated and described herein as

embodied in a program-controlled unit and method for

identifying and/or analyzing errors in program-controlled

units, it is nevertheless not intended to be limited to the

details shown, since various modifications and structural

25 changes may be made therein without departing from the spirit

of the invention and within the scope and range of equivalents

of the claims.

The construction and method of operation of the invention,

5   however, together with additional objects and advantages

thereof will be best understood from the following description

of specific embodiments when read in connection with the

accompanying drawing.

10   Brief Description of the Drawing:

The sole figure of the drawing is a schematic view outlining

the design of a program-controlled unit.

Description of the Preferred Embodiments:

15   The program-controlled unit described here may be a

microprocessor, a microcontroller, a signal processor, or the

like.

Referring now to the sole figure of the drawing in detail,

20   there is illustrated the basic design of the program-

controlled unit under consideration. For the sake of

completeness, it should be understood that the figure shows

only those parts of the program-controlled unit which are of

particular interest in the present case.

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The full design of program-controlled units, the function thereof and the way in which they work are known generally and require no more detailed explanation.

5   The program-controlled unit under consideration can be tested using one or more scan chains. It is distinguished in that, in response to a predetermined event during program execution, it can change to a state in which selected ones or all of the elements which can be connected to form scan chains are no

10   longer able to change their state. If the elements which can be connected to form scan chains are then connected to form one or more scan chains and the latter are read, this produces the states of the scan chain elements at the time of the predetermined event. If the predetermined event represents a

15   malfunction in the program-controlled unit or a shortly preceding or subsequent event, the data read from the scan chains can be used to ascertain and/or analyze the cause of the malfunction.

20   To be able to identify the discrepancies between the data read from the scan chains and the data which would be obtained in the undisturbed normal case, the said data are preferably compared with the corresponding data for a program-controlled unit which does not have the malfunction in question.

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The components of the program-controlled unit which are shown
in the figure comprise a central processing unit CPU, a clock
generator CGU, an On-Chip Debug Support unit OCDS, a JTAG
module JTAG (Joint Test Action Group) and a processor stop

5   unit PSU; selected ones or all of the flip-flops in the
program-controlled unit can be connected to form one or more
scan chains SC.

When the program-controlled unit is operating normally, it, or

10   more precisely its CPU, processes programs which are to be
executed; the data representing the instructions to be
executed at this time are stored in a program memory (not
shown in the figure) provided inside or outside the program-
controlled unit.

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The CPU and the other components of the program-controlled
unit operate with the timing of the clock signals CLOCK
produced by the clock generator CGU.

20   The scan chains SC and the On-Chip Debug Support unit are used
for identifying and/or analyzing hardware and/or software
errors.

The design and operation of scan chains have already been

25   described in detail and require no further explanation.

The task of the On-Chip Debug Support unit is to monitor the occurrence of particular events and to react in a predetermined manner upon the occurrence of the event in question.

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Predetermined events are, by way of example, that the program-controlled unit accesses a particular memory address in the program and/or data store, and/or that the program-controlled unit reads in predetermined data from the program and/or data store or outputs them thereto, and/or that a predetermined register in the program-controlled unit adopts a predetermined content, and/or that other states which can be used as break conditions in debuggers arise. The predetermined event can also be that particular events occur simultaneously or in a particular order or that a particular number of clock cycles has elapsed after the occurrence of a particular event or a particular sequence of events.

Known On-Chip Debug Support units react to the occurrence of the predetermined event by

- signalling the occurrence of the event to an input and/or output connection of the program-controlled unit; and/or

- starting a "monitor program" which can be used to monitor the state and the response of the program-controlled unit exactly; and/or

5   - prompting the program-controlled unit to interrupt or stop the program execution of the program which is actually to be executed, for example by repeatedly executing NOP instructions.

10   In the case of the program-controlled unit considered in more detail in the present case, the OCDS unit is additionally or alternatively able to change the program-controlled unit to a state in which selected ones or all of the elements which can be connected to form scan chains can no longer change their state.

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In the example under consideration, this is achieved by deactivating the clock generator CGU. The discontinuation of the clock signals produced by the clock generator CGU freezes the instantaneous state of those components of the program-

20   controlled unit that are supplied with clock signals by the clock generator CGU.

It will be understood by those skilled in the pertinent art that freezing of the instantaneous states of the elements

which can be connected to form scan chains can also be brought

about in a large variety of other ways.

In the example under consideration, the clock generator CGU

5   supplies the entire program-controlled unit with clock

signals; for this reason, the state of the entire program-

controlled unit is frozen in the present case. However, it

should be pointed out that it is not absolutely necessary to

stop the entire program-controlled unit.

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The clock generator CGU is deactivated using the processor

stop unit PSU; this unit deactivates the clock generator CGU

at the request of the On-Chip Debug Support unit OCDS.

15   When the clock generator CGU has been deactivated, those

components of the program-controlled unit which are normally

supplied with clock signals by the clock generator CGU can no

longer change their state.

20   However, it continues to be possible for the elements which

can be connected to form scan chains to be interconnected to

form one or more scan chains, and to be read.

If this is done, extensive information is obtained about the

25   state of the program-controlled unit at the time at which the

predetermined event detected by the OCDS unit occurred.

The data read from the scan chains are preferably compared with corresponding data for a correctly operating program-controlled unit. The differences ascertained in this process

5   can be used to identify, locate and/or analyze the error in the malfunctioning program-controlled unit quickly and easily.

The On-Chip Debug Support unit OCDS, the processor stop unit PSU and the scan chains SC can be controlled externally (from

10   outside the program-controlled unit) using the JTAG module.

The JTAG module is a known interface and requires no more detailed explanation.

15   The OCDS unit can be notified via the JTAG interface of, among other things,

- whether it needs to monitor the occurrence of predetermined events;

- what the predetermined event is; and/or

20   - how the OCDS unit needs to react to the occurrence of the predetermined event.

The processor stop unit can be notified via the JTAG interface of whether and possibly how it needs to react to requests from the OCDS unit.

5   The scan chains SC can be put together, broken up, read and written to via the JTAG interface.

Hence, all operations which need to be performed in the program-controlled unit for the purposes of identifying and/or

10   analyzing errors in the program-controlled unit in the manner described above can be prompted from outside the program-controlled unit using a standard interface. If the system containing the program-controlled unit is extended accordingly, it is possible to perform error detection and

15   error analysis without having to remove the program-controlled unit from the system containing it.- This is found to be of great advantage, because it allows maximum ease and reliability of error detection and error analysis.

20   The described program-controlled unit and the described method make it possible to identify and analyze errors in program-controlled units quickly and reliably even if they arise only under certain circumstances.